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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,871	12/24/2003	Osamu Sagano	02910.000106.	9351

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EXAMINER	
DINH, DUC Q	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,871	SAGANO ET AL.	
	Examiner	Art Unit	
	DUC Q. DINH	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 6-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 6-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (U.S Patent No. 5,734,361) in view of Sarrasin et al. (U.S Patent No. 5,555,000), hereinafter Sarrasin.

In reference to claim 1, Suzuki discloses in Fig. 8 an image display apparatus comprising:

electron emitting devices arranged in matrix form, driven via a plurality of row wirings and column wirings;

scanning circuit (202) for sequentially selecting and scanning the row wirings (3072:fig. 4);

modulation circuit (209) for outputting a modulated signal to be applied to the column wirings (3073. Fig. 4); and

voltage drop compensation circuit (206, 207, 208 of Fig. 8) for calculating corrected image data for reducing an influence of voltage drops due to at least resistance components of the row wirings, with respect to image data, col.(10, lines 45-51);

wherein the voltage drop compensation circuit includes:

an effective voltage calculating circuit (207) for finding an effective voltage value on the basis of image data, the effective voltage value being a value obtained by average in a time direction a voltage amplitude value of a modulated signal corresponding to the image data for one horizontal scanning period; (see Figures 9, col. 11, lines 59-67 and col. 12, lines 1-28); and

a compensation value calculating circuit (208) for calculating for reducing an influence of voltage drops due to at least resistance components of the row wiring, with respected to the effective voltage value; and

wherein the modulation circuit outputs a modulated signal on the basis of the corrected image data (col. 12, lines 29-49)

Accordingly, Suzuki discloses everything except wherein the modulation circuit generates a modulated signal by modulating both a pulse width and a voltage amplitude.

Sarrasin discloses voltage drop compensation circuit to correct image data for reducing influence of voltage drops due to the resistance of the row wiring (col. 2, lines 45-55) using a modulated signal by modulation both a pulse width and a voltage amplitude as shown in Fig. 1.

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the modulation circuit for outputting modulated signal to by both a pulse width and a voltage amplitude in the display of Suzuki as taught by Sarrasin

because it would permit the selection of large number of grey scale levels for the display device (col. 3, lines 25-30 of Sarrasin)

In reference to claim 6, Suzuki discloses in Figs. 11 the modulated signal has a one voltage amplitude value.

In reference to claim 7, Suzuki discloses everything except the modulation circuit increases a time width of a pulse waveform of the modulated signal by one unit time or a voltage amplitude value of a portion of the pulse waveform of the modulated signal by one unit voltage when input data of the modulation circuit is increased by one unit

Sarrasin discloses wherein the modulation circuit increases a time width of a pulse waveform of the modulated signal by one unit time or a voltage amplitude value of a portion of the pulse waveform of the modulated signal by one unit voltage (V5-V6 of Fig. 1 of Sarrasin), when input data of the modulation circuit is increased by one unit.

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the modulation circuit to provide the desired waveform as taught by Sarrasin in the device of Suzuki because it would provide a display system that have a combination of the advantages of the consumption of digital circuits and the analog addressing method, while permitting the selection of a large number of grey levels. (col. 3, lines 25-30).

In reference to claims 8-9, , Suzuki discloses wherein the voltage drop compensation circuit calculates the corrected image data with respect to image data obtained by multiplying the image data by a gain of greater than 0 but not greater than

1, so that the corrected image is contained in an input range of the modulation circuit. (see Fig. 8-10 and 28)

In reference to claims 10, Suzuki discloses wherein the voltage drop compensation circuit calculates the corrected image data with respect to image data obtained by multiplying the image data by a gain of greater than 0 but not greater than 1, so that the corrected image is contained in an input range of the modulation circuit. (see Fig. 8-10 and 28).

In reference to claims 11-12, refer to the rejections as applied to claims 8-10.

In reference to claims 13, Suzuki discloses wherein the modulation circuit outputs the modulated signal on the basis of limited range-corrected image data obtained by multiplying the corrected image data by a gain of greater than 0 but not greater than 1, so that the limited range-corrected image data is contained in an input range of the modulation circuit. (see Fig. 8-10 and 28).

Response to Arguments

2. Applicant's arguments with respect to claims 1 and 6-13 have been considered but are moot in view of the new ground(s) of rejection and further in view of the personal interview with the Applicant's Representative on July 02, 2008.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DUC Q. DINH whose telephone number is (571)272-7686. The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD HJERPE can be reached on (571)272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Duc Q Dinh/
Examiner, Art Unit 2629